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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/055,499	01/22/2002	Jin-Yuan Lee	JCLA8534	7456

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EXAMINER	
THAI, LUAN C	
ART UNIT	**PAPER NUMBER**
2891	

DATE MAILED: 05/10/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/055,499	LEE ET AL.	
	Examiner	Art Unit	
	Luan Thai	2891	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *15 March 2005*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *204-280* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *204-280* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *22 January 2002* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date ~~3/15/05~~ 11/22/2005
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Request for Continued Examination

1. A request for continued examination under 37 CFR 1.114, including the fee set forth in 37 CFR 1.17(e), was filed in this application after final rejection. Since this application is eligible for continued examination under 37 CFR 1.114, and the fee set forth in 37 CFR 1.17(e) has been timely paid, the finality of the previous Office action has been withdrawn pursuant to 37 CFR 1.114. Applicant's submission filed on 3/15/05 has been entered.

Claim Objections

2. Claim **233** is objected to because of the following informalities:

In claim 1, line 2, "*a die having at a first pad*" should be changed to --*a die having at least a first pad*--.

Appropriate correction is required.

Claim Rejections - 35 USC § 102

3. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

4. Claims 255, 266, and 274 are rejected under 35 U.S.C. 102(b) as being anticipated by Kim et al (6,004,867).

The figures and reference numbers referred to in this office action are used merely to indicate an example of a specific teaching and are not to be taken as limiting.

Regarding claims 255, 266, and 274, Kim et al (see specifically figure 5A-5E) disclose a chip packaging method comprising: joining a die (310) and a substrate (320) (Fig. 5C-5D) by an adhesive (Col. 3, lines 40+); depositing a gold bump (330) over the substrate, and cutting the substrate (Fig. 5E).

Claim Rejections - 35 USC § 103

5. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

6. Claims 204-205, 207-208, 211-213, 216-219, 222-223, 225-226, 228, and 230-232 are rejected under 35 U.S.C. 103(a) as being unpatentable over Eichelberger et al (6,396,148 of record) in view of Marcinkiewicz (6,025,995 of record).

The figures and reference numbers referred to in this office action are used merely to indicate an example of a specific teaching and are not to be taken as limiting.

Regarding claims 204-205, 207-208, 211-213, 216-219, 222-223, 225, 228, and 230-232, Eichelberger et al (see specifically figures 1-7) disclose a chip packaging method comprising: providing a substrate (101) with a surface; providing a plurality of dies (102), wherein each die has an active surface, a backside that is opposite to the active

surface, and a plurality of metal pads (107) located on the active surface, whereas the backside of each die (102) is adhered to the surface of the substrate by an adhesive tape (103); forming a filling layer (104) of polymer or epoxy over the substrate (101) and surrounding the peripheral of the dies (102), wherein a top surface of the filling layer (104) being planar to the active surface of the dies (104) (see figures 3A and 4A); forming a first dielectric layer (106) of polyimide over the top surface of the substrate (101) and over the active surface of the dies (102), and patterning the first dielectric layer (106) to form a plurality of first thru-holes (122) (see figures 3D and 4B); forming a plurality of first patterned lines (108), wherein the first patterned lines (108) is electrically connected to the metal pads (107) of the dies (102) through the first dielectric layer (106), and wherein the first patterned lines (108) has a plurality of first bonding pads electrically connected to solder balls (110). Eichelberger et al further disclose: the method step of forming a patterned passivation layer (109) (or 232) on top of the first dielectric patterned lines (108) (or 206) and exposing the first bonding pads on the first patterned wiring layer (108) for solder balls (110) electrically connected to (as disclosed in figure 1). Eichelberger et al further disclose a step of singularizing the chip package structure to form a single chip package (Col. 8, lines 46+), and that the similar steps as described above can be repeated until all required patterned lines and dielectric layers have been completed (Col. 8, lines 53+). Note that figures 6C-7C also disclose passivation layer (232) is formed on top of the first dielectric patterned wiring layer 206) and exposing the first bonding pads on the first patterned wiring layer (209) for solder

balls (234) electrically connected to. Eichelberger et al., however, do not explicitly teach the substrate comprising an organic material (e.g., polymer).

Marcinkewicz while related to a similar semiconductor structure design teaches the substrate (14) in the integrated circuit module (10) could be made by different kinds materials such as: ceramic, plastic, silicon or any III-V of similar compound, etc., (Col. 3, lines 58+), which are considered as known materials for forming a substrate in semiconductor art. It would have been obvious to one of ordinary skill in the art at the time the invention was made to use a known material, such as plastic (considered as an organic material), to form the substrate in Eichelberger et al.'s chip package, since it has been held to be within the general skill of a worker in the art to select a known material on the basis of its suitability for the intended use as a matter of obvious design choice. Note that plastic (organic material) is considered: as "polyimide resin" (see U.S. Pat. No. 3,677,112, column 3, line 3, to Keniston of record).

Regarding claim 226, the proposed method of Eichelberger et al. and Marcinkiewicz discloses the claimed invention except for the substrate comprising multiple insulation layers being pressured. Although Eichelberger et al. and Marcinkiewicz do not specifying the process of forming the substrate, it would have been obvious to one of ordinary skill in the art at the time the invention was made to form the substrate by a process comprising pressing multiple insulation layers since such process is commonly applied in semiconductor art for making a insulation substrate or board and such application is held to be within the ordinary designing ability expected of a person skilled in the art. Note that applicant has not disclosed that the substrate by pressing multiple insulation layers provides any advantage, is used for a particular purpose, or

solve 'a stated problem. One of ordinary skill in the art, furthermore, would have expected applicant's invention to perform equally well with either processes of forming the insulation substrate because they perform the same function of a base or a carrier for the dies or chips mounted thereon.

7. Claim 206 is rejected under 35 U.S.C. 103(a) as being unpatentable over Eichelberger et al (6,396,148 called "Eic-148" of record) and Marcinkiewicz (6,025,995 of record), as applied to claim 204 above, and further in view of Eichelberger et al (5,841,193, called "Eic-193" of record).

Regarding claim 206, the proposed method of Eic-148 and Marcinkiewicz discloses the claimed invention as detailed above except for not explicitly teaching the dies performing different functions.

Eic-193 while related to a similar chip packaging method teaches that the product formed by such method can comprise different dies (Col. 8, lines 55+). It would have been obvious to one of ordinary skill in the art at the time the invention was made to apply the proposed method of Eic-148 and Marcinkiewicz with the dies performing different functions, since such application is commonly used in the art, as taught by Eic-193, and it is held to be within the ordinary designing ability expected of a person skilled in the art.

8. Claims 233-236, 238-239, 243-244, 247-252, 255-261, 264-268, 271-274 and 276-277, are rejected under 35 U.S.C. 103(a) as being unpatentable over Eichelberger et al (6,396,148 of record) in view of Kim et al. (6,004,867).

Regarding claims 233-236, 238, 243-244, 247-252, 255-261, 264-268, 271-274 and 276, Eichelberger et al. (see specifically figures 1-7) disclose a chip packaging method comprising: providing a substrate (101) with a surface; providing a plurality of dies (102), wherein each die

has an active surface, a backside that is opposite to the active surface, and a plurality of metal pads (107) located on the active surface, whereas the backside of each die (102) is adhered to the surface of the substrate by an adhesive tape (103); forming a filling layer (104) of polymer or epoxy over the substrate (101) and surrounding the peripheral of the dies (102), wherein a top surface of the filling layer (104) being planar to the active surface of the dies (104) (see figures 3A and 4A); forming a first dielectric layer (106) of polyimide over the top surface of the substrate (101) and over the active surface of the dies (102), and patterning the first dielectric layer (106) to form a plurality of first thru-holes (122) (see figures 3D and 4B); forming a plurality of first patterned lines (108), wherein the first patterned lines (108) is electrically connected to the metal pads (107) of the dies (102) through the first dielectric layer (106), and wherein the first patterned lines (108) has a plurality of first bonding pads electrically connected to solder balls (110). Eichelberger et al further disclose: the method step of forming a patterned passivation layer (109) (or 232) on top of the first dielectric patterned lines (108) (or 206) and exposing the first bonding pads on the first patterned wiring layer (108) for solder balls (110) electrically connected to (as disclosed in figure 1). Eichelberger et al further disclose a step of singularizing the chip package structure to form a single chip package (Col. 8, lines 46+), and that the similar steps as described above can be repeated until all required patterned lines and dielectric layers have been completed (Col. 8, lines 53+). Note that figures 6C-7C also disclose passivation layer (232) is formed on top of the first dielectric patterned wiring layer 206) and exposing the first bonding pads on the first patterned wiring layer (209) for solder balls (234) electrically connected to. Eichelberger et al., however, do not explicitly teach the bump comprising gold.

It should be noted that gold is widely used in semiconductor art for forming a bump (called gold bump) since gold bump provides a high electrical conductivity and oxidizing-free. For instance, Kim et al. (Col. 6, lines 59+) disclose the solder bump (330) made of gold. Therefore, it would have been obvious to one of ordinary skill in the art at the time of the invention was made to use the gold bump, as taught by Kim et al, in Eichelberger et al.'s package, in order to provide high electrical conductivity and oxidizing-free.

Regarding claims 239 and 277, the proposed method of Eichelberger et al. and Kim et al discloses the claimed invention except for the substrate comprising multiple insulation layers being pressured. Although Eichelberger et al. and Kim et al. do not specifying the process of forming the substrate, it would have been obvious to one of ordinary skill in the art at the time the invention was made to form the substrate by a process comprising pressing multiple insulation layers since such process is commonly applied in semiconductor art for making a insulation substrate or board and such application is held to be within the ordinary designing ability expected of a person skilled in the art. Note that applicant has not disclosed that the substrate by pressing multiple insulation layers provides any advantage, is used for a particular purpose, or solve 'a stated problem. One of ordinary skill in the art, furthermore, would have expected applicant's invention to perform equally well with either processes of forming the insulation substrate because they perform the same function of a base or a carrier for the dies or chips mounted thereon.

9. Claims 241-242 and 279-280 are rejected under 35 U.S.C. 103(a) as being unpatentable over Eichelberger et al (6,396,148 of record) and Kim et al. (6,004,867), as applied to claims 233-234 and 255, and further in view of Saito et al (5,049,980 of record).

Regarding claims 241-242 and 279-280, the proposed method of Eichelberger et al. and Kim et al. discloses the claimed invention as detailed above except for teaching the substrate comprising: polymer (claims 241 and 279) or thermosetting plastic (claims 242 and 280).

It should be noted that polymer and thermosetting plastic are widely used in semiconductor art for making a substrate, as disclosed by Saito et al. (Col. 2, lines 42+). Therefore, it would have been obvious to one of ordinary skill in the art at the time of the invention was made to use polymer or thermosetting plastic, as taught by Saito et la., to form the substrate in the proposed package of Eichelberger et al. and Kim et al., since such materials are commonly used in the art, and such application of these materials is held to be within the ordinary designing ability expected of a person skilled in the art.

10. Claims 228-229 are rejected under 35 U.S.C. 103(a) as being unpatentable over Eichelberger et al (6,396,148 of record) in view of Marcinkiewicz (6,025,995 of record), as applied to claims 204, and further in view of Saito et al (5,049,980 of record).

Regarding claims 228-229, the proposed method of Eichelberger et al. and Marcinkiewicz discloses the claimed invention as detailed above except for teaching the substrate comprising: polymer (claim 228) or thermosetting plastic (claim 229).

It should be noted that polymer and thermosetting plastic are widely used in semiconductor art for making a substrate, as disclosed by Saito et al. (Col. 2, lines 42+). Therefore, it would have been obvious to one of ordinary skill in the art at the time of the invention was made to use polymer or thermosetting plastic, as taught by Saito et la., to form the substrate in the proposed package of Eichelberger et al. and Marcinkiewicz, since such materials

are commonly used in the art, and such application of these materials is held to be within the ordinary designing ability expected of a person skilled in the art.

11. Claim 224 is rejected under 35 U.S.C. 103(a) as being unpatentable over Eichelberger et al (6,396,148 of record) in view of Marcinkiewicz (6,025,995 of record), as applied to claims 204 and 222, and further in view of Kim et al. (6,004,867).

Regarding claim 224, the proposed method of Eichelberger et al. and Marcinkiewicz discloses the claimed invention as detailed above except for teaching the solder bump comprising gold.

It should be noted that gold is widely used in semiconductor art for forming a bump (called gold bump) since gold bump provides a high electrical conductivity and oxidizing-free. For instance, Kim et al. (Col. 6, lines 59+) disclose the solder bump (330) made of gold. Therefore, it would have been obvious to one of ordinary skill in the art at the time of the invention was made to use the gold bump, as taught by Kim et al, in Marcinkiewicz and Eichelberger et al.'s package, in order to provide high electrical conductivity and oxidizing-free.

12. Claims 209-210 and 227 are rejected under 35 U.S.C. 103(a) as being unpatentable over Eichelberger et al (6,396,148 of record) in view of Marcinkiewicz (6,025,995 of record), as applied to claims 204 and 207-208, and further in view of Fillion et al. (5,353,498).

Regarding claims 209-210, the proposed method of Eichelberger et al. and Marcinkiewicz discloses the claimed invention as detailed above except for teaching the polarizing using the process comprising: etching (claim 209) or grinding (claim 210).

It should be noted that etching or grinding is widely used in semiconductor art for polarizing a surface event that the buffer material has spilled on the substrate or chip, or in the

event that the surfaces are non-planar, as taught by Fillion et al. (Col. 4, lines 54+). It would have been obvious to one of ordinary skill in the art at the time the invention was made to recognize that combining *Fillion et al.'s teachings with* the proposed method of Eichelberger et al. and Marcinkiewicz would have been beneficial because *Fillion et al.'s teachings* help to planarize the surface event that the polymer material has spilled on the chip, or in the event that the surfaces are non-planar.

Regarding claim 227, the proposed method of Eichelberger et al. and Marcinkiewicz discloses the claimed invention as detailed above except for teaching the substrate being formed by a process comprising molding.

Fillion et al. while related to similar MCM forming method teach the substrate (24) being formed by a process comprising molding so that plurality of chips with differing thicknesses can be formed in a module (Col. 2, lines 1+). It would have been obvious to one of ordinary skill in the art at the time the invention was made to recognize that combining the molding process of Fillion with the proposed invention of Eichelberger et al. and Marcinkiewicz would have been beneficial because Fillion's molding process help forming a MCM having plurality of chips with differing thicknesses.

13. Claims 237, 245-246, 269-270 and 275, are rejected under 35 U.S.C. 103(a) as being unpatentable over Eichelberger et al (6,396,148 of record) and Kim et al. (6,004,867), as applied to claims 233-234, 243-244, 255 and 267-268, and further in view of Fillion et al. (5,353,498).

Regarding claims 245-246 and 269-270, the proposed method of Eichelberger et al. and Kim et al. discloses the claimed invention as detailed above except for teaching the polarizing using the process comprising: etching (claims 245 and 269) or grinding (claims 246 and 270).

It should be noted that etching or grinding is widely used in semiconductor art for polarizing a surface event that the buffer material has spilled on the substrate or chip, or in the event that the surfaces are non-planar, as taught by Fillion et al. (Col. 4, lines 54+). It would have been obvious to one of ordinary skill in the art at the time the invention was made to recognize that combining *Fillion et al.'s teachings with* the proposed method of Eichelberger et al. and Kim et al. would have been beneficial because *Fillion et al.'s teachings* help to planarize the surface event that the polymer material has spilled on the chip, or in the event that the surfaces are non-planar.

Regarding claims 237 and 275, the proposed method of Eichelberger et al. and Kim et al. discloses the claimed invention as detailed above except for teaching the substrate being formed by a process comprising molding.

Fillion et al. while related to similar MCM forming method teach the substrate (24) being formed by a process comprising molding so that plurality of chips with differing thicknesses can be formed in a module (Col. 2, lines 1+). It would have been obvious to one of ordinary skill in the art at the time the invention was made to recognize that combining the molding process of Fillion with the proposed invention of Eichelberger et al. and Kim et al. would have been beneficial because Fillion's molding process help forming a MCM having plurality of chips with differing thicknesses.

14. Claims 220-221 are rejected under 35 U.S.C. 103(a) as being unpatentable over Eichelberger et al (6,396,148 of record) in view of Marcinkiewicz (6,025,995 of record), as applied to claim 204, and further in view of Choi (6,428,377 or record).

Regarding claims 220-221, the proposed method of Eichelberger et al. and Marcinkiewicz discloses the claimed invention as detailed above except for forming the patterned lines by: electroplating process (claim 220) or sputtering process (claim 221).

Electroplating and sputtering techniques, however, are two of well-known metal-depositing techniques in semiconductor art, as disclosed by Choi (Col. 7, lines 5-17). It would have been obvious to one of ordinary skill in the art at the time the invention was made to apply the electroplating technique to form the metal patterned lines in the proposed method of Wachtler et al. and Eichelberger et al., since such metal depositing techniques are well known in the art, as taught by Choi, and the applying of such technique is held to be within the ordinary designing ability expected of a person skilled in the art.

15. Claims 253-254 and 262-263 are rejected under 35 U.S.C. 103(a) as being unpatentable over Eichelberger et al (6,396,148 of record) and Kim et al. (6,004,867), as applied to claims 233 and 255-257, and further in view of Choi (6,428,377 or record).

Regarding claims 253-254 and 262-263, the proposed method of Eichelberger et al. and Marcinkiewicz discloses the claimed invention as detailed above except for forming the patterned lines by: electroplating process (claims 253 and 262) or sputtering process (claims 254 and 263).

Electroplating and sputtering techniques, however, are two of well-known metal-depositing techniques in semiconductor art, as disclosed by Choi (Col. 7, lines 5-17). It would have been obvious to one of ordinary skill in the art at the time the invention was made to apply the electroplating technique to form the metal patterned lines in the proposed method of Wachtler et al. and Kim et al., since such metal depositing techniques are well known in the art,

as taught by Choi, and the applying of such technique is held to be within the ordinary designing ability expected of a person skilled in the art.

16. Claim 214 is rejected under 35 U.S.C. 103(a) as being unpatentable over Eichelberger et al (6,396,148 of record) in view of Marcinkiewicz (6,025,995 of record), as applied to claims 204 and 213, and further in view of Tseng (6,395,580).

Regarding claim 214, the proposed method of Eichelberger et al. and Marcinkiewicz discloses the claimed invention as detailed above except for the adhesive comprising conductive paste.

Tseng while related to a similar mounting technique of a die on a substrate teaches that a conductive paste is applied between the die and the substrate in order to improve heat dissipation when the die is in use (Col. 6, lines 61+). It would have been obvious to one of ordinary skill in the art at the time the invention was made to recognize that combining *Tseng's teaching of using conductive paste with* the proposed method of Eichelberger et al. and Kim et al. *invention* would have been beneficial because *Tseng's teaching* helps improve the heat dissipation when the die is in use.

17. Claims 237 and 275 are rejected under 35 U.S.C. 103(a) as being unpatentable over Eichelberger et al (6,396,148 of record) in view of Kim et al. (6,004,867), as applied to claims 233-234, 236, 255 and 274, and further in view of Tseng (6,395,580).

Regarding claims 237 and 275, the proposed method of Eichelberger et al. and Kim et al. discloses the claimed invention as detailed above except for the adhesive comprising conductive paste.

Tseng while related to a similar mounting technique of a die on a substrate teaches that a conductive paste is applied between the die and the substrate in order to improve heat dissipation when the die is in use (Col. 6, lines 61+). It would have been obvious to one of ordinary skill in the art at the time the invention was made to recognize that combining *Tseng's teaching of using the conductive paste with* the proposed method of Eichelberger et al. and Kim et al. *invention* would have been beneficial because *Tseng's teaching* helps improve the heat dissipation when the die is in use.

18. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Luan Thai whose telephone number is 571-272-1935. The examiner can normally be reached on 6:30 AM - 5:00 PM, Monday to Thursday.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Bradley W. Baumeister can be reached on 571-272-1722. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Luan Thai
Primary Examiner
Art Unit 2891
May 6, 2005